MAASAI MARA UNIVERSITY

REGULAR UNIVERSITY EXAMINATIONS
2018/2019 ACADEMIC YEAR
THIRD YEAR *FIRST* SEMESTER

SCHOOL OF SCIENCE
BACHELOR OF SCIENCE

COURSE CODE: PHY 3115

COURSE TITLE: PHYSICS LABORATORY V

DATE: 7TH DECEMBER, 2018 **TIME: 1430-1530 HRS**

INSTRUCTIONS TO CANDIDATES

- Attempt Question **ONE** and any other **TWO**.
- Use of sketch diagrams where necessary and brief illustrations are encouraged.
- Read the instructions on the answer booklet keenly and adhere to them.

QUESTION ONE (20 MARKS)

You are given an Integrated Circuit 74HC00 that contains 4, 2-input logic gates as shown in Fig. 1

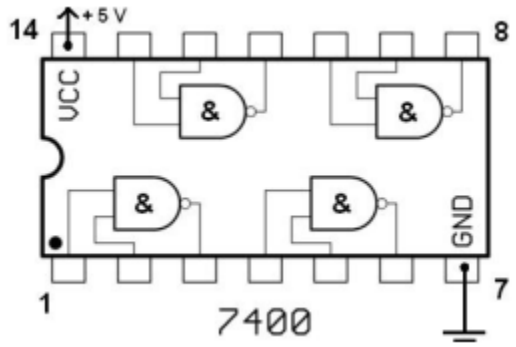

Fig. 1: Pin diagram of IC 74HC00

(a) Identify the logic gate shown in Fig. 1 **(1 mark)**

(b) State the connotation of the following in the identification of the IC;

(i) 74 **(1 mark)**

(ii) HC **(1 mark)**

(iii) 00 **(1 mark)**

(iv) GND **(1 mark)**

(v) VCC **(1 mark)**

(c) The logic gate type shown in Fig. 1 is one of the universal gates.

(i) Briefly explain why it is referred to as a universal gate. **(1 mark)**

(ii) State **ONE** other logic gate that is also universal **(1 mark)**

(iii) State **TWO** advantages of universal gates **(2 marks)**

(d)(i) With an aid of logical diagrams, perform Boolean operations to illustrate how the logic gate type shown in Fig. 1 can implement the function of a 2-input OR gate. **(5 marks)**

(ii) In addition to the IC in Fig. 1, you are provided with a power supply, patch cords and digital voltmeter. On the solderless breadboard shown in Fig. 2,

connect a circuit to implement the 2-input OR gate tasked in part (d)(i) above to generate a high signal. **(5marks)**

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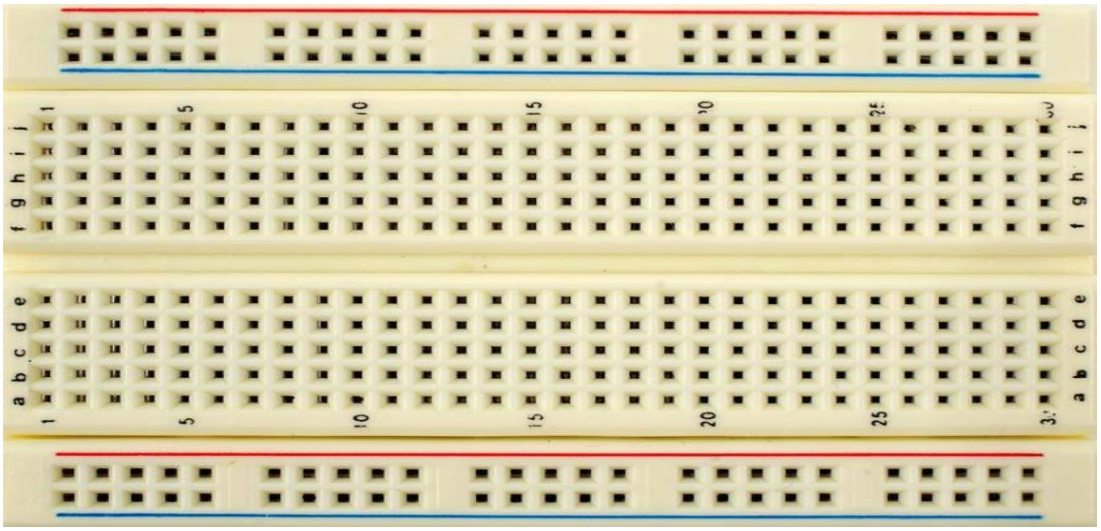

Fig. 2

QUESTION TWO (10 MARKS)

Consider the two circuits shown below in Fig. 3.

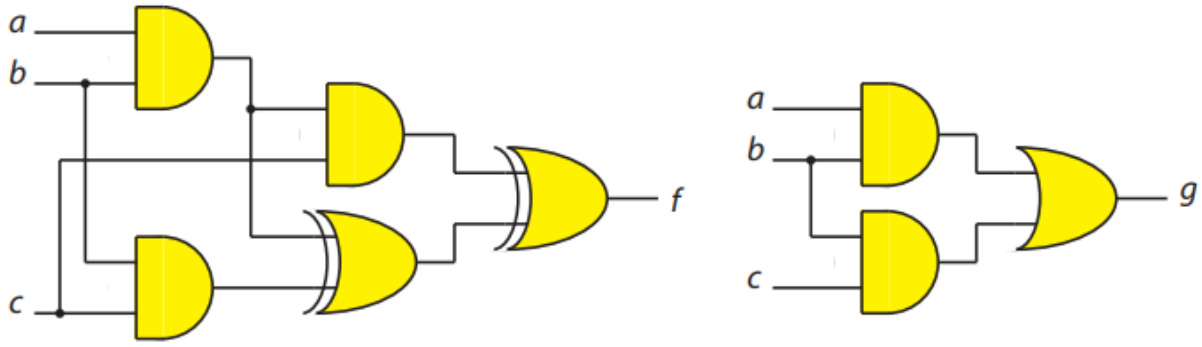

Fig. 3

Prove or disprove that the two circuits given in Fig. 3 implement the same function by employing the following tools:

(a) Algebraic transformations **(4 marks)**

(b) Truth table **(3 marks)**

(c) Karnaugh map **(3 marks)**

QUESTION THREE (10 MARKS)

An engine has 3 fail-safe sensors. The engine should keep running unless any of the following conditions arise:

(i) If sensor 2 is activated.

(ii) If sensor 1 and sensor 3 are activated at the same time

(iii) If sensor 2 and sensor 3 are activated at the same time

Derive the truth table for this system

Hint: Let A = Sensor1 B=Sensor2 C=Sensor3

F=Engine Shutdown=0, Engine Running=1 **(10 marks)**

QUESTION FOUR (10 MARKS)

Fig. 4 is a logic diagram of a half-adder. The sum and carry operations are implemented by the IC 7408N and 7486N.

(a)With the aid of a truth table, state which IC implements the following operations:

(i)Carry **(2 marks)**

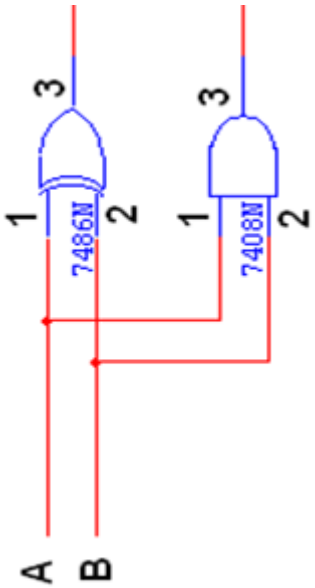

Fig. 4

(ii)Sum **(2 marks)**

(b)In a practical session, you are tasked to construct a half-adder as shown in Fig. 4. You realize that ICs 7408N and 7486N are lacking but only ICs 74HC00 (see in Fig. 1) are provided. Can this practical be successful? Explain your answer using relevant logic diagrams. **(5 marks)**

(c)State the limitation of half-adder **(1 mark)**